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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,491	10/30/2003	Ross E. Johnson	ROC920030025US1	8050

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EXAMINER	
INGBERG, TODD D	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,491	JOHNSON, ROSS E.	
	Examiner	Art Unit	
	Todd Ingberg	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 31 have been examined.

Information Disclosure Statement

1. The Information Disclosure Statement filed October 30,2003 has been considered.

Drawings

2. The Drawings filed October 30,2003 has been accepted.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 30 and 31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are directed to a signal directly or indirectly by claiming a medium and the Specification recites evidence where the computer readable medium is define as a "***wave***" (such as a carrier wave) . In that event, the claims are directed to a form of energy which at present the office feels does not fall into a category of invention. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf

5. Claims 7 – 9 and 12 – 14 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. The limitations under the scope of claims 1, 3,4 and 5 are not concrete. As claimed the optimization is to computer programs where the optimization randomly reorders. This will produce non-deterministic results. Please, note this rejection was not raised in later

claim sets because the limitations present in the independent claim (e.g. claim 17). NO art rejection applied to claims 7-9 and 12 – 14 because they are not concrete.

Claim 7– No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 5, wherein testing the subset of orderings includes randomly selecting a different ordering after testing an ordering from the subset of orderings.

Claim 8– No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 7, wherein randomly selecting the different ordering comprises swapping two program code segments in a previous ordering.

Claim 9– No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 8, wherein the program code segments each comprise a module, and wherein randomly selecting the different ordering further comprises constraining selection of the two program code segments to modules in the same replaceable unit destination.

Claim 12 – No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises accepting a change to an ordering if a calculated cost for such ordering is lower than that of a working ordering.

Claim 13 – No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises randomly accepting a change to an ordering even if the calculated cost for such ordering is not lower than that of the working ordering.

Claim 14 – No art rejection – Not considered Concrete under 35 U.S.C.§ 101
The method of claim 11, wherein selecting an ordering from among the plurality of orderings further comprises prematurely halting the testing of orderings based upon a halt criterion.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-4, 10-11, 15-16, 17, 19 and 24-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Enhanced Simulated Annealing for Automatic Reconfiguration of Multiprocessors in Space by James R. Slagle et al, ACM 1989 (referred to as **Path**).

Claim 1
Path anticipates a method of ordering program code in a computer memory (Path, Abstract, reconfiguration), the method comprising: selecting an ordering from among a plurality of orderings for a plurality of program code segments using a heuristic algorithm (Path, pages 403 – 404, standard deviation section on); and ordering the plurality of program code segments in a memory of a computer using the selected ordering (Path, page 401 – multiprocessor space).

Claim 3
The method of claim 1, wherein the heuristic algorithm comprises a simulated annealing algorithm. (Path, page 405 bottom right to 407)

Claim 4
The method of claim 3, wherein selecting the ordering using the heuristic algorithm includes testing a subset of the plurality of orderings. (Path, page 404, Left side number of iterations).

Claim 10
The method of claim 3, wherein selecting an ordering from among the plurality of orderings comprises testing a subset of orderings at each of a plurality of temperature values. (Path, pages 403 to 404, determination based on temperature).

Claim 11
The method of claim 10, wherein selecting an ordering from among the plurality of orderings further comprises testing a subset of orderings at each temperature value (Path, page 404 to 405).

Claim 15
The method of claim 1, wherein the program code segments each comprise a module from an operating system kernel. (Path, page 402, 2 The Application).

Claim 16
The method of claim 15, wherein each module comprises a high use module, and wherein selecting the ordering from among a plurality of orderings comprises generating a high use module list. (Path, pages 403 to 404, determination based on temperature).

Claim 17
Path anticipates a n apparatus, comprising: a processor; and program code configured to be executed by the processor to optimize execution of program code (As per claim 1)in a computer of the type including a multi-level memory architecture (Path, page 402, hierarchy) by using a

heuristic algorithm to select an ordering (As per claim 1) from among a plurality of orderings for a plurality of program code segments in the program code (As per claim 1).

Claim 19
The apparatus of claim 17, wherein the heuristic algorithm comprises a simulated annealing algorithm. (Path, page 403, standard deviation and calculating cost and page 405 bottom right to 407).

Claim 24
The apparatus of claim 19, wherein the program code is configured to select an ordering from among the plurality of orderings by testing a subset of orderings at each of a plurality of temperature values, and testing a subset of orderings at each temperature value. (Path, pages 403 to 404, determination based on temperature).

Claim 25
The apparatus of claim 24, wherein the program code is configured to select an ordering from among the plurality of orderings by accepting a change to an ordering if a calculated cost for such ordering is lower than that of a working ordering. (Path, page 403, Right side).

Claim 26
The apparatus of claim 25, wherein the program code is configured to select an ordering from among the plurality of orderings by randomly accepting a change to an ordering even if the calculated cost for such ordering is not lower than that of the working ordering. (Path, page 401, "Random").

Claim 27
The apparatus of claim 17, wherein the program code is configured to select an ordering from among the plurality of orderings by prematurely halting the testing of orderings based upon a halt criterion. (Path, page 404, section 5.1.3 Determining the Stopping Criteria).

Claim 28
The apparatus of claim 17, wherein the program code segments each comprise a module from an operating system kernel. (Path, page 402, 2 The Application).

Claim 29
The apparatus of claim 28, wherein each module comprises a high use module, and wherein the program code is configured to select the ordering from among a plurality of orderings by generating a high use module list. (Path, pages 403 to 404, determination based on temperature).

Claim 30
Path anticipates a program product, comprising: first program code configured to optimize execution of second program code in a computer of the type including a multi-level memory architecture (Path, page 402, hierarchy) by using a heuristic algorithm to select an ordering (As per claim 1) from among a plurality of orderings for a plurality of program code segments in the

second program code (As per claim 1); and a signal bearing medium bearing the first program code (Path, page 401, MIN – right side).

Claim 31
The program product of claim 30, wherein the signal bearing medium includes at least one of a recordable medium and a transmission medium. (Path, page 401, MIN – right side).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 5 – 6, 18 and 20 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enhanced Simulated Annealing for Automatic Reconfiguration of Multiprocessors in Space by James R. Slagle et al, ACM 1989 (referred to as **Path**) in view of USPN #6971,092 B1 Chillimbi issued November 29, 2005 and filed August 24, 2001 (referred to as **Cache**).

Motivation to Combine Path and Cache
Path teaches the heuristic based optimization of simulated annealing of program Paths. What Path does not explicitly mention is the relationship of path optimization and the use of cache. It is Cache who teaches optimizing the use of Cache. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine Path and Cache, because optimization of programs makes programs run more efficient.

Claim 2
The method of claim 1, wherein the heuristic algorithm (as per claim 1) is configured to minimize cache misses in the computer (Cache, Col 1, Background Section).

Claim 5
The method of claim 4, wherein testing the subset of the plurality of orderings includes, for each ordering in the subset, calculating a cost for such ordering (Path, page 403, standard deviation and calculating cost and page 405 bottom right to 407) based upon cache miss rates for such ordering (Cache, col 7, lines 5 - 17).

Claim 6
The method of claim 5, wherein calculating the cost for each ordering comprises calculating a plurality of hits/reference values, misses/address values, and misses/entry values (Cache, col 9, line 65 to col 10, line 12).

Claim 18
The apparatus of claim 17, wherein the heuristic algorithm is configured to minimize cache misses in the computer. As per claim 5.

Claim 20
The apparatus of claim 19, wherein the program code is configured to select the ordering using the heuristic algorithm by testing a subset of the plurality of orderings (As per claim 1), and wherein the program code is configured to test the subset of the plurality of orderings by, for each ordering in the subset (As per claim 4), calculating a cost for such ordering based upon cache miss rates for such ordering (As per claim 5).

Claim 21
The apparatus of claim 20, wherein the program code is configured to test the subset of orderings by randomly selecting a different ordering (Path, page 401, 1. Introduction) after testing an ordering from the subset of orderings (Path, page 404, Number of determined iterations).

Claim 22
The apparatus of claim 21, wherein the program code is configured to randomly select the different ordering by swapping two program code segments in a previous ordering. (Path, page 401 bottom right – swap).

Claim 23
The apparatus of claim 22, wherein the program code segments each comprise a module, and wherein the program code is configured to randomly select the different ordering by constraining selection of the two program code segments to modules in the same replaceable unit destination. (Path, page 401, Introduction).

Correspondence Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Todd Ingberg whose telephone number is (571) 272-3723. The examiner can normally be reached on during the work week..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Todd Ingberg
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TI